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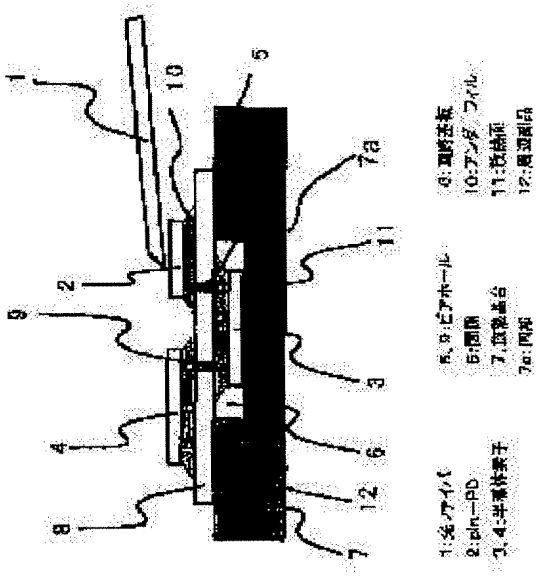
(54) SEMICONDUCTOR DEVICE-PACKAGING DEVICE AND OPTICAL COMMUNICATION DEVICE

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a packaging device that is compact and has improved cooling effect in a device for mounting an optical semiconductor device and a semiconductor device on a circuit board.
SOLUTION: A pin-PD2 is electrically connected onto a circuit board 8 and is fixed by an underfill 10 and is packaged at a side opposite to the packaging surface of the pin-PD2 of the circuit board 8 of a next-stage preamplifier IC 3. Also, a signal line is electrically connected by a via hole 8 that is provided in the circuit board 8. Also, the signal line is connected to a next-stage semiconductor IC 4 by a via hole 9 in the circuit board 8. Especially, the preamplifier IC 3 is arranged in a gap 6 that is provided on a radiation substrate 7 for fixing the circuit board 8, and a radiation surface 11 of the preampfifier IC 3 is electrically connected to the radiation substrate 7 that also plays a role of electrical ground.



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* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
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CLAIMS

[Claim(s)]
[Claim 1] The heat dissipation pedestal which has a crevice, and the circuit board prepared on said heat dissipation pedestal so that said crevice might be covered at least, It has at least two semiconductor devices which said circuit board reached on the other hand, and were mounted at least one [at a time] in both the principal planes of another side, respectively. Said semiconductor device which while joins to said heat dissipation pedestal of said circuit board, and was mounted in the principal plane is semiconductor device mounting equipment which is arranged in said crevice and joined with sufficient thermal conductivity to said a part of crevice [at least].
[Claim 2] Said semiconductor device is semiconductor device mounting equipment [equipped with the optical fiber or optical waveguide for outputting and inputting light to said OPTO semiconductor device] according to claim 1 including at least one OPTO semiconductor device.
[Claim 3] Said OPTO semiconductor device is semiconductor device mounting equipment according to claim 2 connected with said semiconductor device which is mounted in the principal plane of another side which is not joined to said heat dissipation pedestal of said circuit board, and has been arranged in said crevice.
[Claim 4] Said OPTO semiconductor device is semiconductor device mounting equipment according to claim 2 with which it is mounted in the principal plane of another side which is not joined to said heat dissipation pedestal of said circuit board, and said all semiconductor devices other than said OPTO semiconductor device are arranged in said crevice.
[Claim 5] Said semiconductor device which while joins to said heat dissipation pedestal of said circuit board, and was mounted in the principal plane, and said a part of crevice are semiconductor device mounting equipment according to claim 1 or 2 currently fixed with thermally conductive resin.
[Claim 6] Said semiconductor device and said circuit board are semiconductor device mounting equipment according to claim 1 or 2 electrically connected by conductive resin.
[Claim 7] It is semi-conductor mounting equipment according to claim 1 or 2 with which some of the dielectric constants differ from the dielectric constant of other parts in said circuit board.
[Claim 8] Some [said] dielectric constants of said circuit board are larger semiconductor device mounting equipment according to claim 7 than the dielectric constant of said circuit board.
[Claim 9] Said circuit board is semiconductor device mounting equipment according to claim 7 which has multilayer structure and has the ingredient with which dielectric constants differ mutually between layers at least.
[Claim 10] For the ingredient with which it has the independent electrode arranged at the principal plane of said another side, some electrodes of said semiconductor device are mounted in said independent electrode, and said independent electrode and said dielectric constant differ from each other, said circuit board is semiconductor device mounting equipment according to claim 9 which forms the capacitor in the interior of said circuit board.
[Claim 11] It is semiconductor device mounting equipment according to claim 10 by which the electrode of said semiconductor device is the current supply terminal or bias terminal to this semiconductor device, and said independent electrode is connected with a ground.

[Claim 12] It is semiconductor device mounting equipment according to claim 1 or 2 which said circuit board has the beer hall which penetrates both the principal plane, and is electrically connected in the distance for said circuit board thickness when at least two semiconductor devices of said circuit board which reach on the other hand and are mounted in the principal plane of another side mind said beer hall.
[Claim 13] Said optical waveguide or optical fiber is semiconductor device mounting equipment according to claim 2 formed in the interior of said circuit board.
[Claim 14] Semiconductor device mounting equipment according to claim 2 with which the 1st guide slot or marker for positioning said optical fiber is prepared in said heat dissipation pedestal.

[Claim 15] Semiconductor device mounting equipment according to claim 2 with which the 2nd guide slot for arranging said optical waveguide or said optical fiber is established in said circuit board.
[Claim 16] Said semiconductor device mounted on said circuit board or said semiconductor device and an optical fiber, or optical waveguide is semiconductor device mounting equipment according to claim 1 or 2 by which mold is carried out with insulating resin.
[Claim 17] Said circuit board and said heat dissipation pedestal are semiconductor device mounting equipment according to claim 1 by which connection immobilization is carried out with conductive resin.
[Claim 18] Said optical fiber or optical waveguide is semiconductor device mounting equipment according to claim 2 or 13 which has aslant incidence or the reflective structure which carries out outgoing radiation, and is optically combined with said OPTO semiconductor device in light to the direction of a guided wave of light.
[Claim 19] Optical-communication equipment which either of claims 1-18 is equipped with semiconductor device mounting equipment, a modulation means or a recovery means, and the transmitting means or receiving means of a publication, and can be used as an optical sending set or an optical receiving set.

[Translation done.]

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the semiconductor device mounting equipment which is applied to the optical transceiver circuit in optical communication and which mounted the OPTO semiconductor device and the semiconductor device in the circuit board.
[0002]
[Description of the Prior Art] In optic fiber communication, when application to CATV or mobile communications is considered, the property of transmitting an analog signal in a high-speed broadband is demanded of the optical transceiver section. The equipment which contains the semiconductor device which outputs and inputs a RF electrical signal to the semiconductor device in the OPTO semiconductor device list connected to an optical fiber is used for optical communication.
[0003] A conventional optical semi-conductor and semiconductor device mounting equipment are shown in drawing 5 . Here, an optical receiving set is described. an optical fiber — 100 — from — light — slanting — polish — an end face — from — light-receiving — a function — having — an OPTO semiconductor device — it is — a photodiode — (— PD —) — 200 — incidence — carrying out . The signal by which light and electric conversion were carried out by PD200 is inputted into the semiconductor device 300 which has the front-end magnification function which amplifies with a low noise, and a signal is amplified. And a signal is led to the semiconductor device 400 of the next step, and signal processing is performed.
[0004] OPTO semiconductor device (PD) 200, a semiconductor device 300,400 and the circumference components 122, and 132 are mounted on the same side of the RF circuit board 80, and arrangement immobilization is carried out on the case pedestal 70. Here, OPTO semiconductor device 100 and the semiconductor device 200-300 are performing flip chip mounting (FCB) which used under-filling 1000.
[0005]
[Problem(s) to be Solved by the Invention] With the above configurations, even if under-filling is not used for the distance between an adjacent OPTO semiconductor device and a semiconductor device in order to prevent the lap of under-filling, it is necessary to separate it from the need for reservation of the mounting tooth space between circumference components 0.3mm or more, for example. However, on the other hand, it is desirable between an OPTO semiconductor device and the semiconductor device of the next step to approach as much as possible and to arrange.
[0006] Moreover, although it is necessary to prepare a heat dissipation device in a semiconductor device in order to radiate heat efficiently since the semiconductor device which has a magnification function generates heat, with the above-mentioned configuration, a heat dissipation device will be prepared in the top face of a semiconductor device with a drawing, and arrangement may become complicated.
[0007] Moreover, although the technique of radiating heat in a semiconductor device by preparing only the hole where a semiconductor device goes into the RF circuit board 80, making a semiconductor device inside-out, arranging on the case pedestal 70, and connecting with the

RF circuit board 80 electrically by wire bonding, although a drawing does not show is also performed Since this differs from the mounting approach of an OPTO semiconductor device, in an actual production process, it must stop newly having to introduce the production facility which performs the different mounting technique from the mounting approach of an OPTO semiconductor device, and may push up the cost of semiconductor device mounting equipment as a result.
[0008] The purpose is offering the semiconductor device mounting equipment which it approaches as much as possible, and the mounting arrangement of an OPTO semiconductor device and the semiconductor device can be carried out by making this invention in view of the above-mentioned technical problem, and can radiate heat effectively in a semiconductor device, can unify a mounting process in addition, and can attain a miniaturization, and the optical-communication equipment using it.
[0009]
[Means for Solving the Problem] In order to attain the above-mentioned purpose, the 1st this invention (it corresponds to claim 1) The heat dissipation pedestal which has a crevice, and the circuit board prepared on said heat dissipation pedestal so that said crevice might be covered at least, It has at least two semiconductor devices which said circuit board reached on the other hand, and were mounted at least one [at a time] in both the principal planes of another side, respectively. While joins to said heat dissipation pedestal of said circuit board, and said semiconductor device mounted in the principal plane is semiconductor device mounting equipment which is arranged in said crevice and joined with sufficient thermal conductivity to said a part of crevice [at least].
[0010] Moreover, the 2nd this invention (it corresponds to claim 2) is above-mentioned this invention equipped with an optical fiber or optical waveguide for said semiconductor device to output and input light to said OPTO semiconductor device including at least one OPTO semiconductor device.
[0011] Moreover, said OPTO semiconductor device is mounted in the principal plane of another side which is not joined to said heat dissipation pedestal of said circuit board, and the 3rd this invention (it corresponds to claim 3) is above-mentioned this invention connected with said semiconductor device arranged in said crevice.
[0012] Moreover, the 4th this invention (it corresponds to claim 4) is mounted in the principal plane of another side which does not join said OPTO semiconductor device to said heat dissipation pedestal of said circuit board, and said all semiconductor devices other than said OPTO semiconductor device are above-mentioned this inventions arranged in said crevice.
[0013] Moreover, while joins the 5th this invention (it corresponds to claim 5) to said heat dissipation pedestal of said circuit board, and said semiconductor device mounted in the principal plane and said a part of crevice are above-mentioned this inventions currently fixed with thermally conductive resin.
[0014] Moreover, the 6th this invention (it corresponds to claim 6) is above-mentioned this invention to which said semiconductor device and said circuit board are electrically connected by conductive resin.
[0015] Moreover, the 7th this invention (it corresponds to claim 7) is above-mentioned this invention in which some of the dielectric constants differ from the dielectric constant of other parts in said circuit board.
[0016] Moreover, the 8th this invention (it corresponds to claim 8) is above-mentioned this invention with some [said] larger dielectric constants of said circuit board than the dielectric constant of said circuit board.
[0017] Moreover, the 9th this invention (it corresponds to claim 9) is above-mentioned this invention which said circuit board has multilayer structure and has the ingredient with which dielectric constants differ mutually between layers at least.
[0018] Moreover, said circuit board of the 10th this invention (it corresponds to claim 10) is [the ingredient with which it has the independent electrode arranged at the principal plane of said another side, some electrodes of said semiconductor device are mounted in said independent electrode, and said independent electrode and said dielectric constant differ from each other]

above-mentioned this invention which forms the capacitor in the interior of said circuit board.
[0019] Moreover, the electrode of said semiconductor device is the current supply terminal or bias terminal to this semiconductor device, and the 11th this invention (it corresponds to claim 11) is above-mentioned this invention by which said independent electrode is connected with a ground.
[0020] Moreover, it has the beer hall where, as for the 12th this invention (it corresponds to claim 12), said circuit board penetrates both the principal plane, and at least two semiconductor devices of said circuit board which reaches on the other hand and are mounted in the principal plane of another side are above-mentioned this inventions electrically connected in the distance for said circuit board thickness by minding said beer hall.
[0021] Moreover, for said optical waveguide or optical fiber, the 13th this invention (it corresponds to claim 13) is semiconductor device mounting equipment according to claim 2 formed in the interior of said circuit board.
[0022] Moreover, the 14th this invention (it corresponds to claim 14) is above-mentioned this invention by which the 1st guide slot or marker for positioning said optical fiber is prepared in said heat dissipation pedestal.
[0023] Moreover, the 15th this invention (it corresponds to claim 15) is above-mentioned this invention by which the 2nd guide slot for arranging said optical waveguide or said optical fiber is established in said circuit board.
[0024] Moreover, said semiconductor device by which the 16th this invention (it corresponds to claim 16) is mounted on said circuit board or said semiconductor device and an optical fiber, or optical waveguide is above-mentioned this invention by which mold is carried out with insulating resin.
[0025] Moreover, the 17th this invention (it corresponds to claim 17) is above-mentioned this invention by which connection immobilization of said circuit board and said heat dissipation pedestal is carried out with conductive resin.
[0026] Moreover, the 18th this invention (it corresponds to claim 18) is above-mentioned this invention by which said optical fiber or optical waveguide has aslant incidence or the reflective structure which carries out outgoing radiation, and it combines light with said OPTO semiconductor device optically to the direction of a guided wave of light.
[0027] Moreover, the 19th this invention (it corresponds to claim 19) is optical-communication equipment which it has semiconductor device mounting equipment, a modulation means or a recovery means, and one of the 1st to 18th transmitting means or receiving means of this invention, and can be used as an optical sending set or an optical receiving set.
[0028] Above this inventions approach, connect an OPTO semiconductor device and a semiconductor device electrically, and do not degrade a RF property, and can radiate heat effectively in a semiconductor device. However, an OPTO semiconductor device is vocabulary which generally puts the light emitting device or photo detector which consists of semi-conductors, such as semiconductor laser, LED, and a photodiode, here, and the compound device containing a light emitting device and a photo detector is also included further. Although an OPTO semiconductor device is the same configuration as a semiconductor device, the part which outputs and inputs light is located in the electrode side of a semiconductor device, its rear face, or a side face.
[0029]
[Embodiment of the Invention] Hereafter, the operation gestalt of this invention is explained with reference to an attached drawing. In addition, in a drawing, the same reference designator puts a same or equivalent thing.
[0030] (Gestalt 1 of operation) Drawing 1 shows the semiconductor device mounting equipment of the gestalt 1 of operation of this invention. An OPTO semiconductor device is a photo detector like the pin photodiode (following pin-PD) 2 here, and light carries out incidence to pin-PD2 from the slanting polished surface of an optical fiber 1. On the circuit board 8, solder or conductive resin connects electrically and pin-PD2 is fixed by under-filling 10.
[0031] With the component side of pin-PD2 of the circuit board 8, pre amplifier IC 3 of the next step is mounted in the opposite side, and is fixed by under-filling 10. Furthermore, the signal line

of pre amplifier IC 3 is electrically connected by the beer hall 5 prepared in the circuit board 8. Furthermore, a signal line is connected also with the semiconductor IC 4 of the next step by the beer hall 9 in the circuit board 8. Especially the pre amplifier IC 3 is arranged in the gap 6 formed by a part of circuit board 8 exposed in crevice 7a prepared in the heat dissipation pedestal 7 which fixes the circuit board 8, and said crevice 7a, and the heat sinking plane 11 of pre amplifier IC 3 and the heat dissipation pedestal 7 which serves as an electric ground have composition thermally connected through crevice 7a.
[0032] Since a property will be changed if influenced of light, in order to avoid this effect, as for that by which a semiconductor device like pre amplifier IC 3 as the 1st condition on which a semiconductor device and an OPTO semiconductor device operate good here was created, for example by gallium arsenide etc. depending on that presentation, it is desirable to detach an OPTO semiconductor device and to arrange. Moreover, since an OPTO semiconductor device conversely like pin-PD2 tends to be influenced of heat, it is desirable to separate from the heat source and the semiconductor device which can change like pre amplifier IC 3, and to arrange.
[0033] It is more desirable to arrange from the point which raises a RF property, so that pin-PD2 and pre amplifier IC 3 may approach, and to take a short path cord as the 2nd condition, on the other hand, in the high frequency band (for example, 1GHz or more, desirably 5GHz or more) where a semiconductor device operates.
[0034] Like the conventional example, when filling one side of the two above-mentioned conditions with the configuration which arranges an OPTO semiconductor device and a semiconductor device on the same side of the same circuit board, with it, another side was not to be filled, but with it, it is separated by the circuit board 8 while the gestalt of this operation has connected pre amplifier IC 3 with pin-PD2 electrically on both sides of the circuit board 8 in the beer hall 9 in between.
[0035] Therefore, since about two pin-PD [which has effect disadvantageous for pre amplifier IC 3] light, and the heat from the pre amplifier IC 3 which has effect disadvantageous for pin-PD2 approach mutually and are arranged by having minded the beer hall 9 while they will all be interrupted by the circuit board 8, a short path cord can be taken and it becomes possible to raise a RF property. Moreover, since the part and pre amplifier IC 3 of crevice 7a which were formed in the heat dissipation pedestal 7 are connected thermally, the heat dissipation property of pre amplifier IC 3 is improving.
[0036] While being able to remove the effect of heat to the effect of the light to the semiconductor device arranged by approaching while according to the semiconductor device mounting equipment by the gestalt of this operation approaching more and have arranged the OPTO semiconductor device and the semiconductor device, unifying a mounting process by having considered as the above configurations using the mounting approach of the conventional OPTO semiconductor device, and an OPTO semiconductor device, a semiconductor device can be made to radiate heat efficiently.
[0037] In addition, in the above-mentioned configuration, although it fills up with under-filling 10 and the pre amplifier IC 3 and the circuit board 8 which are arranged in pin-PD2, a semiconductor IC 4, and crevice 7a explained as that to which both are being fixed by this Under-filling 10 is excluded and you may make it fix the pre amplifier IC 3 and the circuit board 8 which are arranged in a semiconductor IC 4 and crevice 7a only by the member which performs electrical installation, as shown in drawing 7 . In this case, the effect of the dielectric constant which under-filling 10 has can be removed, and the RF property of a semiconductor device can be raised further.
[0038] Moreover, if a gap 6 is also filled up with under-filling 66 and pre amplifier IC 3 is fixed in crevice 7a as shown in drawing 8 , it will become possible to raise further the heat dissipation property of pre amplifier IC 3. What is necessary is it to be desirable to have good thermal conductivity as for under-filling 66, for example, just to use gel and thermally conductive resin at this time.
[0039] Moreover, in the above-mentioned explanation, although pre amplifier IC 3 explained as what is thermally connected with the heat dissipation pedestal 7 on the base of crevice 7a, it may be made to be connected on a side face to others. That the semiconductor device of this

invention is arranged in a crevice, and should just be joined with sufficient thermal conductivity to said a part of crevice [at least] in short, as long as there is the part in a crevice, it may be any part.
[0040] (Gestalt 2 of operation) Drawing 2 shows the semiconductor device mounting equipment of the gestalt 2 of operation of this invention. The semiconductor IC 4 of a different point from the gestalt 1 of operation is the point which mounted the circumference components 12 and 13 mounted in the circumference of ICs, such as a capacitor, in the substrate side of the opposite side where pin-PD2 is mounted, and has been connected by beer halls 9 and 16 while being mounted on the same field as the component side of pre amplifier IC 3 in the circuit board 8 and performing I/O of a signal on this substrate side.
[0041] By the beer hall 14, the signal output from a semiconductor IC 4 can be drawn and taken out on the front face of the circuit board 8. Although the heat sinking plane 11 of pre amplifier IC 3 and the heat sinking plane 15 of a semiconductor IC 3 have composition thermally connected by the heat dissipation pedestal 7, this configuration is the effective mounting technique in the case of IC in which febrility has a semiconductor IC 4 like postamplifier or signal processing IC. Furthermore, like the gestalt 1 of operation, even if it is the case where it is that in which a semiconductor IC 4 tends to receive the effect of light, such as a product made from gallium arsenide, in addition to pre amplifier IC 3, it can abolish being influenced of about two pin-PD light.
[0042] Even if pin-PD2 and pre amplifier IC 3 consider the electrolyte thickness of a component the case of a substrate with a thickness of less than 1mm, for example, the alumina ceramic substrate of 0.3mm thickness, in the circuit board 8, a signal line will be connected in a short distance of less than at least 500 micrometers.
[0043] As the mounting approach of pin-PD2 (OPTO semiconductor device) to the circuit board 8, pre amplifier IC, and a semiconductor IC (semiconductor device), it is good at the connection method by solder or electroconductive glue. Component mounting by electroconductive glue can ease the stress by the difference in the coefficient of thermal expansion of a component and the circuit board.
[0044] Thus, according to the semiconductor device mounting equipment of the gestalt of this operation, by mounting an OPTO semiconductor device and semiconductor devices, such as pre amplifier IC, in circuit board both sides, and connecting thermally to a heat dissipation case the semiconductor device which connects a signal line electrically and generates heat between this substrate, since the component mounting effectiveness on the circuit board is raised and heat dissipation can also be performed effectively, the miniaturization of equipment can be attained. Furthermore, it becomes possible to shade completely the semiconductor device which is easy to be influenced of light.
[0045] Furthermore, circumference components can be approached and mounted rather than the case where arrangement mounting is carried out, on the same side by carrying out arrangement mounting of the components of each other [the circuit board] which should be arranged around a semiconductor device and its semiconductor device in an opposite field. Especially this is effective when it mounts the capacitor for the high frequency decoupling by the side of a power source by the case where a semiconductor device has high-speed responsibility.
[0046] (Gestalt 3 of operation) Drawing 3 shows the semiconductor device mounting equipment of the gestalt 3 of operation of this invention. Different points from the gestalt 1 of operation shown in drawing 1 are the point that optical waveguide 102 is formed in that substrate, the point of having the optical fiber 101 optically connected with this optical waveguide 102, and a point that the light-receiving side of pin-PD21 is established toward the inside 7, i.e., heat dissipation pedestal, of a substrate component side, in the circuit board 81.
[0047] In this case, the under-filling 10 formed in pin-PD21 needs to use transparent resin, for example, silicon system gel etc. Or it is good also as a configuration which excluded under-filling 10. In drawing 3 , optical waveguide 102 has a total reflection function in the location located in the light-receiving side of pin-PD21, reflects light upwards with a drawing, and leads light to the light-receiving side of pin-PD21. Moreover, to also form the circuit board 81 with the transparent ingredient, for example, what is necessary is just a textile-glass-yarn ingredient. A

guide slot like a V groove or a concave is formed on the circuit board 81, and you may make it arrange optical waveguide 102 into this guide slot at this time.
[0048] Thus, according to the semiconductor device mounting equipment of the gestalt of this operation, by considering as the configuration in which the optical coupling system to an OPTO semiconductor device is made to build in the circuit board, the positioning marker whom optical adjustment with an optical fiber and pin-PD mounts can perform, and compaction of an equipment making process can be aimed at.
[0049] In addition, in fixing an optical fiber 101 to the heat dissipation pedestal 7, the marker and fiber fixed slot at the time of fixing the circuit board 81 which has optical waveguide 102 on the heat dissipation pedestal 7, if a guide slot like a V groove or a concave is formed can be made to use also [pedestal / 7 / heat dissipation], and adjustment immobilization becomes easy.
[0050] In addition, in the above-mentioned explanation, the guide slot formed in the heat dissipation pedestal 7 is equivalent to the 1st guide slot on this invention, and the guide slot formed in the circuit board 81 is equivalent to the 2nd guide slot on this invention.
[0051] (Gestalt 4 of operation) Drawing 4 shows the semiconductor device mounting equipment of the gestalt 4 of operation of this invention. A different point from the gestalt 2 of operation shown in drawing 2 instead of arranging the circumference components 12 and 13 on the circuit board It has the fields 120 and 130 which were embedded and were formed in the circuit board 82 so that an ingredient with specific inductive capacity higher than the ingredient of the circuit board 82 might be exposed on the front face of the circuit board 82, and the field 141 formed with the same ingredient also as the component side of pin-PD2. the field of a longitudinal direction where these fields 120,130,141 counter -- a conductor -- it has a form inserted with an electrode and is the point of having given the function of a capacitor with the field and the electrode.
[0052] This capacitor is electrically connected to pin-PD2, pre amplifier IC 3, and the power-source (bias) supply terminal of a semiconductor IC 4, and especially since it connects with the ground, another conductor of a capacitor is effective in the decoupling of a high frequency field. If there is 100 more than specific inductive capacity in the high dielectric constant ingredient to embed with an alumina or the ceramic ingredient of textile glass yarn, it can be used for it as a capacitor with a capacity of several pF or more by configuration like drawing 4 in the field (stratification plane product) of 0.1mm of bed depths, and 1mm angle.
[0053] Furthermore, if a high dielectric constant ingredient, for example, the ingredient with which specific inductive capacity exceeds 1000, is used, in case the capacitor of the same capacity will be formed by the same thickness, it is possible to make an embedding field small. Moreover, since a capacitor with a large (1000pF or more) capacity can also be formed, coupling in a low frequency field is also realizable by the capacitor of a substrate embedding mold.
[0054] Some examples of a configuration of the electrode the dielectric embedded at the circuit board of the gestalt of this operation and whose dielectric layer of its drawing 6 pinches here are shown. The dielectric layer 150 is embedded in the surface section of the circuit board 190, and the configuration shown in drawing 6 (a) is formed so that the dielectric layer 150 of electrodes 160 and 161 may be pinched. Beer halls 180 and 181 are connected with the electrode 161 and the pattern on the rear face of the circuit board.
[0055] If one side of this beer hall is connected to the bias supply pin of a semiconductor device 3, another side is connected to the bias section on circuit board 82 rear face and an electrode 160 is connected to the ground on a circuit board front face as shown also in drawing 4 , the dielectric layer 150 pinched by electrodes 160 and 161 will function as a capacitor.
[0056] As an example of a configuration of the gestalt of this operation, a dielectric layer 151 is the example currently formed in the inner layer of the circuit board 191, and drawing 6 (b) can have a function as a capacitor like the example shown in drawing 6 (a) by connecting respectively the beer halls 182 and 183 connected with electrodes 162 and 163 and the pattern on the surface of the circuit board 191 in this case. With this configuration, since there is no dielectric layer on the surface of the circuit board 191, there is effectiveness which can carry out formation arrangement of components and the pattern near the beer halls 182 and 183.
[0057] Moreover, drawing 6 (c) is the configuration of connecting the electrode of one of the two

of a capacitor to both sides of the circuit board by the electrode 165 and beer hall 184 where the beer hall connected to an electrode 161 by drawing 6 (a) did not form on the same side of the circuit board, but extended from the dielectric layer 152, and the beer hall 185. Thereby, the circuit of for example, a bias feed zone can be formed on the front face of the circuit board 192.
[0058] Next, drawing 6 (d) is an example of a configuration which counters and arranges two or more electrodes 167, and 168 and 169 to a part of large dielectric layer 153. Thereby, another capacitor can be first formed by the dielectric layer 153 into which one capacitor is inserted with an electrode 167 and an electrode 169 by the dielectric layer pinched with an electrode 167 and an electrode 168. Many capacitors can be formed if an electrode is formed of course still in juxtaposition. In the example of drawing 6 (d), the electrode 167 is used as a common electrode of two capacitor ability, and if this part is connected to a ground, it can use as a capacitor for decoupling. If an electrode 167 is separated and formed for every part, of course, it can use as a capacitor which carried out mutually-independent. Since capacity can be changed by the thickness and area size of a dielectric layer, by using as a substrate for RF circuits especially, reduction of transmission-line capacity can be aimed at with the miniaturization of equipment, and after component mounting can secure the RF property desired.
[0059] In addition, in the gestalt of each operation shown in drawing 4 , drawing 7 , and drawing 8 from drawing 1 , although pin-PD which is a photo detector as an example of the OPTO semiconductor device of this invention was shown, an avalanche photodiode (APD) is sufficient as this. Moreover, semiconductor laser may be used as an OPTO semiconductor device. In order to apply to the example shown here, it is desirable to use semiconductor laser with a small radiation angle with a surface-emitting type. In this case, since it becomes a laser driver IC and generation of heat becomes large more, this configuration of pre amplifier IC 2 which can perform direct heat dissipation to a case is effective.
[0060] Moreover, in the gestalt of each above-mentioned implementation, although explained as a configuration equipped with the semiconductor device and the OPTO semiconductor device, this invention is good also as a configuration which has only a semiconductor device. In this case, it becomes possible to raise heat dissipation effectiveness and mounting effectiveness.
[0061] Moreover, to connection immobilization with the circuit boards 8, 81, and 82 and the heat dissipation pedestal 7, positive electrical installation is possible by the immobilization or solder immobilization by metal ****.
[0062] When anxious about the stress impression to the connection fixed part by the difference in the coefficient of thermal expansion of the circuit boards 8, 81, and 82 and the heat dissipation pedestal 7 furthermore, connection stability may be able to be planned by the stress relaxation in a resin layer by connection which used electroconductive glue.
[0063] Moreover, since the optical fiber and optical waveguide which are mounted in the circuit boards 8, 81, and 82, the OPTO semiconductor device, and the semiconductor device are mounted with sufficient heat dissipation nature, even if they perform a configuration (not shown) which carries out mold altogether with insulating resin, they do not have heat stagnation, and they can prevent mixing of the dust from the outside etc., and can secure long term stability of operation.
[0064] Moreover, what is necessary is for what can secure sufficient touch-down to be desirable, and for the ingredient which was excellent even if it was in both conductive [, such as a metal,] and thermally conductive to be desirable, for example, just to use copper, aluminum, etc. as an ingredient of the heat dissipation pedestal 7, in order to raise a RF property.
[0065] moreover, in using a ceramic substrate as an ingredient of the circuit boards 8 and 81 and 82 grades In order to amend the difference in the coefficient of thermal expansion between the circuit board and a heat dissipation pedestal, covar is arranged on the front face (plane of composition with the circuit boards 8, 81, and 82) of the heat dissipation pedestal 7. What is necessary is just to make it connect with extent which it is made to make this absorb the strain based on the difference in an expansion coefficient, or does not check the thermal conductivity between the circuit board and a heat dissipation pedestal through thin conductive resin.
[0066] In addition, the optical-communication equipment made to constitute from the optical receiving set or the optical sending set using the above-mentioned mounting equipment While

excelling in the heat dissipation effectiveness, and a heat sinking plane product's increasing substantially from the ability of a heat dissipation pedestal to be united with a case and being able to enlarge the heat dissipation effectiveness more When it has a modulation means and a transmitting means, it has the effectiveness which can be miniaturized as an optical transmitter and optical-communication equipment which operates as optical receivers when it has a recovery means and a receiving means.
[0067]
[Effect of the Invention] By mounting a semiconductor device in circuit board both sides, and considering as the configuration which connects thermally to a heat dissipation case the semiconductor device which connects a signal line electrically and generates heat between this substrate, since this invention constituted as mentioned above raises the component mounting effectiveness on the circuit board and can also perform heat dissipation effectively, it can attain the miniaturization of equipment.
[0068] By carrying out arrangement mounting of the components of each other [the circuit board] which should furthermore be arranged around a semiconductor device and its semiconductor device in an opposite field, or embedding a dielectric layer on the circuit board or in the circuit board, and connecting an electrode, the component-mounting effectiveness on the circuit board of the same area is gathered, and it can miniaturize further as equipment. Especially this is effective when it mounts the capacitor for the high frequency decoupling by the side of a power source by the case where a semiconductor device has high-speed responsibility.

[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] The diagrammatic sectional view of the semiconductor device mounting equipment of the gestalt 1 of operation of this invention
[Drawing 2] The diagrammatic sectional view of the semiconductor device mounting equipment of the gestalt 2 of operation of this invention
[Drawing 3] The diagrammatic sectional view of the semiconductor device mounting equipment of the gestalt 3 of operation of this invention
[Drawing 4] The diagrammatic sectional view of the semiconductor device mounting equipment of the gestalt 5 of operation of this invention
[Drawing 5] The diagrammatic sectional view of conventional semiconductor device mounting equipment
[Drawing 6] The diagrammatic sectional view showing the example of a configuration of the dielectric layer embedding circuit board
[Drawing 7] The diagrammatic sectional view showing other examples of a configuration of the semiconductor device mounting equipment of the gestalt 1 of operation of this invention
[Drawing 8] The diagrammatic sectional view showing other examples of a configuration of the semiconductor device mounting equipment of the gestalt 1 of operation of this invention
[Description of Notations]
1,101 Optical fiber
2 pin-PD
3 Four Semiconductor device
5, 9, 14, 16 Beer hall
8 81 Circuit board
7 Heat Dissipation Pedestal
7a Crevice
102 Optical Waveguide
120 130 Dielectric layer

[Translation done.]

SEMICONDUCTOR DEVICE-PACKAGING DEVICE AND OPTICAL COMMUNICATION DEVICE

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Inventor: IIDA MASANORI; ASAKURA HIROYUKI
Applicant: MATSUSHITA ELECTRIC IND CO LTD
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- European:
Application number: JP20010081575 20010321
Priority number(s): JP20010081575 20010321; JP20000084006 20000324

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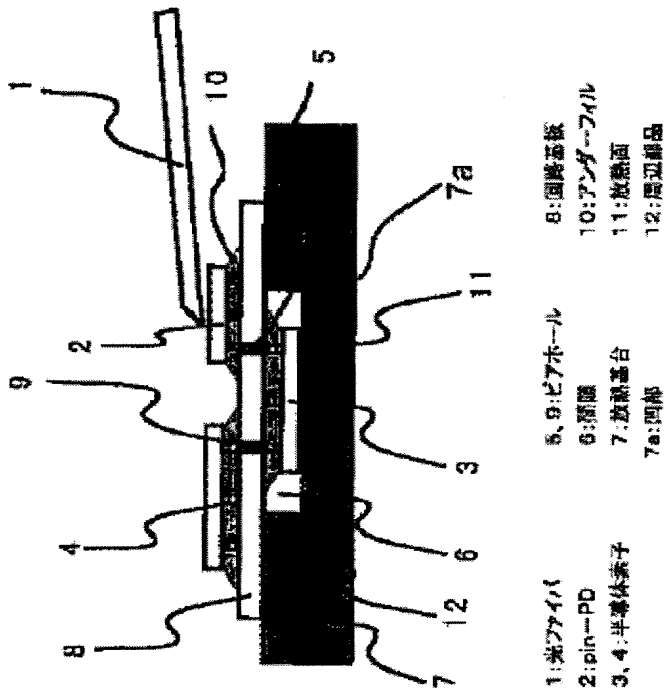
Abstract of **JP2001339077**

PROBLEM TO BE SOLVED: To provide a packaging device that is compact and has improved cooling effect in a device for mounting an optical semiconductor device and a semiconductor device on a circuit board. SOLUTION: A pin-PD2 is electrically connected onto a circuit board 8 and is fixed by an underfill 10 and is packaged at a side opposite to the packaging surface of the pin-PD2 of the circuit board 8 of a next-stage preamplifier IC 3. Also, a signal line is electrically connected by a via hole 8 that is provided in the circuit board 8. Also, the signal line is connected to a next-stage semiconductor IC 4 by a via hole 9 in the circuit board 8. Especially, the preamplifier IC 3 is arranged in a gap 6 that is provided on a radiation substrate 7 for fixing the circuit board 8, and a radiation surface 11 of the preampfifier IC 3 is electrically connected to the radiation substrate 7 that also plays a role of electrical ground.



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Ｈ０１Ｓ　5/022			Ｃ	
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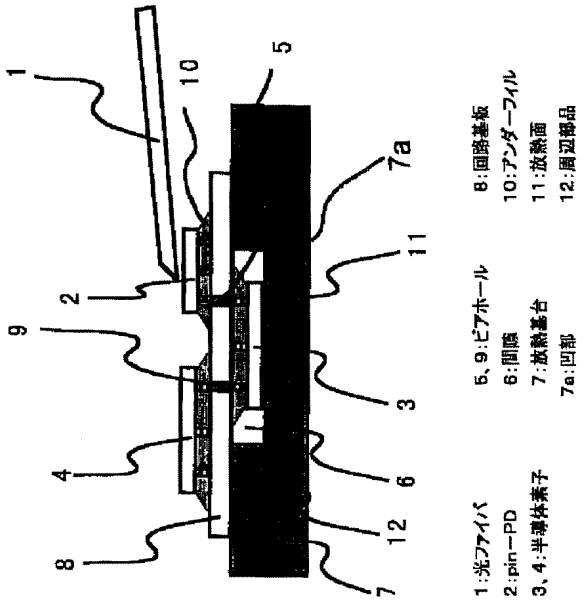
(54)【発明の名称】　半導体素子実装装置および光通信装置

(57)【要約】
【課題】　光半導体素子及び半導体素子を回路基板上に実装した装置において、小型で放熱効果に優れた実装装置を提供する。
【解決手段】　ｐｉｎ－ＰＤ２は回路基板８上に電気的に接続されアンダーフィル１０によって固定され、次段のプリアンプＩＣ３は回路基板８の、ｐｉｎ－ＰＤ２の実装面とは反対側に実装され、かつ信号ラインは回路基板８内に設けられたビアホール８によって電気的に接続される。さらに次段の半導体ＩＣ４とも回路基板８内のビアホール９によって信号ラインは接続される。特にプリアンプＩＣ３は回路基板８を固定する放熱基台７に設けられた間隙６内に配置され、プリアンプＩＣ３の放熱面１１と電気的なグラウンドを兼ねる放熱基台７とが熱的に接続される。



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【特許請求の範囲】

【請求項１】　凹部を有する放熱基台と、
少なくとも前記凹部を覆うように前記放熱基台上に設けられた回路基板と、
前記回路基板の一方および他方の両主面にそれぞれ少なくとも１つづつ実装された少なくとも２つの半導体素子とを備え、
前記回路基板の前記放熱基台と接合する一方の主面に実装された前記半導体素子は、前記凹部内に配置され、前記凹部の少なくとも一部と熱伝導性よく接合されている半導体素子実装装置。

【請求項２】　前記半導体素子は、少なくとも１つの光半導体素子を含むものであり、
前記光半導体素子に対し光を入出力するための光ファイバまたは光導波路を備えた請求項１に記載の半導体素子実装装置。

【請求項３】　前記光半導体素子は、前記回路基板の前記放熱基台と接合しない他方の主面に実装されており、前記凹部に配置された前記半導体素子と接続されている請求項２に記載の半導体素子実装装置。

【請求項４】　前記光半導体素子は、前記回路基板の前記放熱基台と接合しない他方の主面に実装されており、前記光半導体素子以外の全ての前記半導体素子が、前記凹部内に配置されている請求項２に記載の半導体素子実装装置。

【請求項５】　前記回路基板の前記放熱基台と接合する一方の主面に実装された前記半導体素子と前記凹部の一部とは、熱伝導性樹脂により固定されている請求項１または２に記載の半導体素子実装装置。

【請求項６】　前記半導体素子と前記回路基板とは、導電性樹脂により電気的に接続されている請求項１または２に記載の半導体素子実装装置。

【請求項７】　前記回路基板において、その一部分の誘電率は、他の部分の誘電率と異なる請求項１または２に記載の半導体実装装置。

【請求項８】　前記回路基板の前記一部の誘電率は、前記回路基板の誘電率よりも大きい請求項７に記載の半導体素子実装装置。

【請求項９】　前記回路基板は多層構造を有しており、少なくとも層間に互いに誘電率の異なる材料を有する請求項７に記載の半導体素子実装装置。

【請求項１０】　前記回路基板は、前記他方の主面に配置された独立電極を有し、
前記独立電極には、前記半導体素子の電極の一部が実装され、
前記独立電極と前記誘電率の異なる材料とは、前記回路基板の内部にコンデンサを形成している請求項９に記載の半導体素子実装装置。

【請求項１１】　前記半導体素子の電極は、該半導体素子への電源供給端子またはバイアス端子であり、

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前記独立電極はグラウンドと接続される請求項１０に記載の半導体素子実装装置。

【請求項１２】　前記回路基板は、その両主面を貫通するビアホールを有し、
前記回路基板の一方および他方の主面に実装される少なくとも２つの半導体素子は、前記ビアホールを介することにより、前記回路基板厚み分の距離で電気的に接続される請求項１または２に記載の半導体素子実装装置。

【請求項１３】　前記光導波路または光ファイバは、前記回路基板の内部に設けられている請求項２に記載の半導体素子実装装置。

【請求項１４】　前記放熱基台には、前記光ファイバを位置決めするための第１のガイド溝またはマーカが設けられている請求項２に記載の半導体素子実装装置。

【請求項１５】　前記回路基板には、前記光導波路または前記光ファイバを配置するための第２のガイド溝が設けられている請求項２に記載の半導体素子実装装置。

【請求項１６】　前記回路基板上に実装される前記半導体素子、または前記半導体素子および光ファイバまたは光導波路は、絶縁性樹脂によってモールドされている請求項１または２に記載の半導体素子実装装置。

【請求項１７】　前記回路基板と前記放熱基台とは、導電性樹脂により接続固定されている請求項１に記載の半導体素子実装装置。

【請求項１８】　前記光ファイバまたは光導波路は光の導波方向に対して斜めに光を入射または出射する反射構造を有するものであり、前記光半導体素子と光学的に結合されている請求項２または１３に記載の半導体素子実装装置。

【請求項１９】　請求項１から１８のいずれかに記載の半導体素子実装装置と、
変調手段または復調手段と、
送信手段または受信手段とを備え、
光送信装置または光受信装置として用いることが可能な光通信装置。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、光通信における光送受信回路に適用される、光半導体素子や半導体素子を回路基板に実装した半導体素子実装装置に関する。

【０００２】

【従来の技術】光ファイバ通信において、ＣＡＴＶや移動体通信への適用を考えた場合、光送受信部にはアナログ信号を高速広帯域で伝送する特性が要求されている。光ファイバーに接続される光半導体素子並びにその半導体素子に高周波電気信号を入出力する半導体素子を含む装置が、光通信に使用されている。

【０００３】図５に従来の光半導体及び半導体素子実装装置を示す。ここでは光受信装置について述べる。光ファイバ１００からの光は斜め研磨端面から受光機能を有

する光半導体素子であるフォトダイオード（ＰＤ）２００に入射する。ＰＤ２００で光・電気変換された信号は低雑音で増幅を行う前置増幅機能を有する半導体素子３００に入力され、信号は増幅される。そして次段の半導体素子４００に信号が導かれ信号処理を行う。

【０００４】光半導体素子（ＰＤ）２００、半導体素子３００，４００及び周辺部品１２２・１３２は高周波回路基板８０の同一面上に実装され、筐体基台７０上に配置固定される。ここでは光半導体素子１００、半導体素子２００・３００はアンダーフィル１０００を用いたフリップチップ実装（ＦＣＢ）を行っている。

【０００５】

【発明が解決しようとする課題】上記のような構成では、隣り合う光半導体素子及び半導体素子間の距離は、アンダーフィルの重なりを防ぐためや、たとえアンダーフィルを使用しなくても周辺部品の実装スペースの確保の必要性から、例えば０．３ｍｍ以上離す必要がある。しかしながら、その一方で、光半導体素子と次段の半導体素子との間は出来るだけ近接して配置することが望ましい。

【０００６】また、増幅機能を有する半導体素子は発熱するため、効率的に放熱を行うために放熱機構を半導体素子に設ける必要があるが、上記の構成では放熱機構は図面で半導体素子の上面に設けることになり、配置が複雑になる可能性がある。

【０００７】また、図面では示さないが、高周波回路基板８０に半導体素子が入るだけの穴を設け、半導体素子を裏返しにして筐体基台７０上に配置し、ワイヤーボンディングで高周波回路基板８０と電気的に接続することによって、半導体素子の放熱を行う手法も行われているが、これは光半導体素子の実装方法と異なるため、実際の製造工程において、光半導体素子の実装方法とは異なる実装手法を行う生産設備を新たに導入せねばならなくなり、結果的に半導体素子実装装置のコストを押し上げる可能性がある。

【０００８】本発明は、上記の課題に鑑みてなされたものであり、その目的は、光半導体素子及び半導体素子を出来るだけ近接して実装配置でき、かつ半導体素子の放熱を効果的に行え、加えて実装工程を一元化でき、小型化が図れる半導体素子実装装置およびそれを用いた光通信装置を提供することである。

【０００９】

【課題を解決するための手段】上記の目的を達成するために、第１の本発明（請求項１に対応）は、凹部を有する放熱基台と、少なくとも前記凹部を覆うように前記放熱基台上に設けられた回路基板と、前記回路基板の一方および他方の両主面にそれぞれ少なくとも１つづつ実装された少なくとも２つの半導体素子とを備え、前記回路基板の前記放熱基台と接合する一方の主面に実装された前記半導体素子は、前記凹部内に配置され、前記凹部の少なくとも一部と熱伝導性よく接合されている半導体素子実装装置である。

【００１０】また、第２の本発明（請求項２に対応）は、前記半導体素子は、少なくとも１つの光半導体素子を含むものであり、前記光半導体素子に対し光を入出力するための光ファイバまたは光導波路を備えた上記本発明である。

【００１１】また、第３の本発明（請求項３に対応）は、前記光半導体素子は、前記回路基板の前記放熱基台と接合しない他方の主面に実装されており、前記凹部に配置された前記半導体素子と接続されている上記本発明である。

【００１２】また、第４の本発明（請求項４に対応）は、前記光半導体素子は、前記回路基板の前記放熱基台と接合しない他方の主面に実装されており、前記光半導体素子以外の全ての前記半導体素子が、前記凹部内に配置されている上記本発明である。

【００１３】また、第５の本発明（請求項５に対応）は、前記回路基板の前記放熱基台と接合する一方の主面に実装された前記半導体素子と前記凹部の一部とは、熱伝導性樹脂により固定されている上記本発明である。

【００１４】また、第６の本発明（請求項６に対応）は、前記半導体素子と前記回路基板とは、導電性樹脂により電気的に接続されている上記本発明である。

【００１５】また、第７の本発明（請求項７に対応）は、前記回路基板において、その一部分の誘電率は、他の部分の誘電率と異なる上記本発明である。

【００１６】また、第８の本発明（請求項８に対応）は、前記回路基板の前記一部の誘電率は、前記回路基板の誘電率よりも大きい上記本発明である。

【００１７】また、第９の本発明（請求項９に対応）は、前記回路基板は多層構造を有しており、少なくとも層間に互いに誘電率の異なる材料を有する上記本発明である。

【００１８】また、第１０の本発明（請求項１０に対応）は、前記回路基板は、前記他方の主面に配置された独立電極を有し、前記独立電極には、前記半導体素子の電極の一部が実装され、前記独立電極と前記誘電率の異なる材料とは、前記回路基板の内部にコンデンサを形成している上記本発明である。

【００１９】また、第１１の本発明（請求項１１に対応）は、前記半導体素子の電極は、該半導体素子への電源供給端子またはバイアス端子であり、前記独立電極はグラウンドと接続される上記本発明である。

【００２０】また、第１２の本発明（請求項１２に対応）は、前記回路基板は、その両主面を貫通するビアホールを有し、前記回路基板の一方および他方の主面に実装される少なくとも２つの半導体素子は、前記ビアホールを介することにより、前記回路基板厚み分の距離で電気的に接続される上記本発明である。

【００２１】また、第１３の本発明（請求項１３に対応）は、前記光導波路または光ファイバは、前記回路基板の内部に設けられている請求項２に記載の半導体素子実装装置。

【００２２】また、第１４の本発明（請求項１４に対応）は、前記放熱基台には、前記光ファイバを位置決めするための第１のガイド溝またはマーカが設けられている上記本発明である。

【００２３】また、第１５の本発明（請求項１５に対応）は、前記回路基板には、前記光導波路または前記光ファイバを配置するための第２のガイド溝が設けられている上記本発明である。

【００２４】また、第１６の本発明（請求項１６に対応）は、前記回路基板上に実装される前記半導体素子、または前記半導体素子および光ファイバまたは光導波路は、絶縁性樹脂によってモールドされている上記本発明である。

【００２５】また、第１７の本発明（請求項１７に対応）は、前記回路基板と前記放熱基台とは、導電性樹脂により接続固定されている上記本発明である。

【００２６】また、第１８の本発明（請求項１８に対応）は、前記光ファイバまたは光導波路は光の導波方向に対して斜めに光を入射または出射する反射構造を有するものであり、前記光半導体素子と光学的に結合されている上記本発明である。

【００２７】また、第１９の本発明（請求項１９に対応）は、第１から第１８のいずれかの本発明の半導体素子実装装置と、変調手段または復調手段と、送信手段または受信手段とを備え、光送信装置または光受信装置として用いることが可能な光通信装置である。

【００２８】以上のような本発明は、光半導体素子と半導体素子を近接して電気的に接続し高周波特性を劣化させることが無く、また半導体素子の放熱を効果的に行える。ただし、ここで光半導体素子とは、一般に、半導体レーザ、ＬＥＤ、フォトダイオードなどの半導体からなる発光素子または受光素子をさす用語であり、さらに、発光素子及び受光素子を含む複合素子も含む。光半導体素子は半導体素子と同様な形状であるが光の入出力を行う部位が半導体素子の電極側もしくはその裏面あるいは側面に位置するものである。

【００２９】

【発明の実施の形態】以下、添付の図面を参照して本発明の実施形態について説明する。なお、図面において同一の参照記号は、同一または同等のものをさす。

【００３０】（実施の形態１）図１は、本発明の実施の形態１の半導体素子実装装置を示している。光半導体素子は、ここではピン・フォトダイオード（以下ｐｉｎ－ＰＤ）２のような受光素子であり、光ファイバ１の斜め研磨面から光がｐｉｎ－ＰＤ２に入射する。ｐｉｎ－ＰＤ２は回路基板８上に半田または導電性樹脂により電気的に接続されアンダーフィル１０によって固定される。

【００３１】次段のプリアンプＩＣ３は回路基板８の、ｐｉｎ－ＰＤ２の実装面とは反対側に実装され、アンダーフィル１０によって固定される。さらにプリアンプＩＣ３の信号ラインは回路基板８内に設けられたビアホール５によって電気的に接続される。さらに次段の半導体ＩＣ４とも回路基板８内のビアホール９によって信号ラインは接続される。特にプリアンプＩＣ３は回路基板８を固定する放熱基台７に設けられた凹部７ａおよび前記凹部７ａ内に露出した回路基板８の一部によって形成される間隙６内に配置され、プリアンプＩＣ３の放熱面１１と電気的なグラウンドを兼ねる放熱基台７とが、凹部７ａを介して熱的に接続される構成となっている。

【００３２】ここで、半導体素子と光半導体素子とが良好に動作する第１の条件として、プリアンプＩＣ３のような半導体素子は、その組成によっては、例えばガリウム砒素などで作成されたものは光の影響を受けると特性が変動するため、この影響を避けるためには、光半導体素子とは離して配置するのが望ましい。また、逆にｐｉｎ－ＰＤ２のような光半導体素子は、熱の影響を受けやすいため、プリアンプＩＣ３のような、熱源と成りうる半導体素子からは離して配置するのが望ましい。

【００３３】一方、第２の条件として、半導体素子が動作する高周波帯域（例えば１ＧＨｚ以上、望ましくは５ＧＨｚ以上）において、高周波特性を向上させる点からは、ｐｉｎ－ＰＤ２とプリアンプＩＣ３とは、近接するよう配置して、接続線を短くとる方が望ましい。

【００３４】従来例のように、同一回路基板の同一面上に光半導体素子および半導体素子を配置する構成では、上記２つの条件の一方を満たせば他方が満たされないことになっていたが、本実施の形態は、プリアンプＩＣ３は、回路基板８を間に挟んでｐｉｎ－ＰＤ２とビアホール９にて電気的に接続しているとともに、回路基板８によって隔てられている。

【００３５】したがって、プリアンプＩＣ３にとって不利な影響を与えるｐｉｎ－ＰＤ２近傍の光、およびｐｉｎ－ＰＤ２にとって不利な影響を与えるプリアンプＩＣ３からの熱は回路基板８によっていずれも遮られていることとなる一方、ビアホール９を介したことによって互いに近接して配置されるため、接続線を短くとれ、高周波特性を向上させることが可能となる。また、放熱基台７に設けられた凹部７ａの一部とプリアンプＩＣ３とが熱的に接続されているために、プリアンプＩＣ３の放熱特性が向上している。

【００３６】本実施の形態による半導体素子実装装置によれば、以上のような構成としたことにより、従来の光半導体素子の実装方法を用いて、実装工程を一元化したままで、光半導体素子と半導体素子とをより近接して配置できるとともに、近接して配置された半導体素子に対する光の影響、および光半導体素子に対する熱の影響を

取り除くことができるとともに、半導体素子を効率よく放熱させることができる。

【００３７】なお、上記の構成においては、ｐｉｎ－ＰＤ２、半導体ＩＣ４および凹部７ａ内に配置されているプリアンプＩＣ３と回路基板８とは、アンダーフィル１０が充填されており、これにより両者が固定されているものとして説明を行ったが、図７に示すように、アンダーフィル１０を省いて、電気的接続を行う部材のみで半導体ＩＣ４および凹部７ａ内に配置されているプリアンプＩＣ３と回路基板８とを固定するようにしてもよい。この場合、アンダーフィル１０の有する誘電率の影響を取り除いて、半導体素子の高周波特性をさらに向上させることができる。

【００３８】また、図８に示すように、凹部７ａにおいて、間隙６にもアンダーフィル６６を充填してプリアンプＩＣ３を固定するようにすれば、プリアンプＩＣ３の放熱特性をさらに向上させることが可能となる。このとき、アンダーフィル６６は、良好な熱伝導性を有するのが望ましく、例えばゲルや熱伝導性樹脂を用いればよい。

【００３９】また、上記の説明においては、プリアンプＩＣ３は凹部７ａの底面にて放熱基台７と熱的に接続されるものとして説明を行ったが、他に側面にて接続されるようにしてもよい。要するに、本発明の半導体素子は、凹部内に配置され、前記凹部の少なくとも一部に熱伝導性よく接合されていればよく、その一部は凹部内で有ればどの部分であってもよい。

【００４０】（実施の形態２）図２は、本発明の実施の形態２の半導体素子実装装置を示している。実施の形態１と異なる点は、半導体ＩＣ４が、回路基板８において、プリアンプＩＣ３の実装面と同じ面上に実装され、この基板面上で信号の入出力が行われると共に、コンデンサ等のＩＣ周りに実装される周辺部品１２、１３を、ｐｉｎ－ＰＤ２が実装されている反対側の基板面に実装し、ビアホール９、１６によって接続している点である。

【００４１】半導体ＩＣ４からの信号出力は例えばビアホール１４により、回路基板８の表面に導き出し取り出すことが出来る。プリアンプＩＣ３の放熱面１１と半導体ＩＣ３の放熱面１５は放熱基台７で熱的に接続される構成となっているが、この構成は半導体ＩＣ４がポストアンプや信号処理ＩＣのように発熱性のあるＩＣの場合に有効な実装手法である。さらに、実施の形態１と同様、プリアンプＩＣ３に加えて、半導体ＩＣ４がガリウム砒素製など、光の影響を受けやすいものである場合であっても、ｐｉｎ－ＰＤ２近傍の光の影響を受けることをなくすことができる。

【００４２】回路基板８は厚み１ｍｍ以内の基板、例えば０．３ｍｍ厚のアルミナセラミック基板の場合、ｐｉｎ－ＰＤ２とプリアンプＩＣ３とは素子の電極厚を加味しても少なくとも５００μｍ以内の短い距離で信号ラインが接続されることになる。

【００４３】回路基板８へのｐｉｎ－ＰＤ２（光半導体素子）、プリアンプＩＣおよび半導体ＩＣ（半導体素子）の実装方法としては、半田あるいは導電性接着剤による接続方法でよい。導電性接着剤による素子実装の方が、素子と回路基板の熱膨張係数の差異による応力を緩和できる。

【００４４】このように、本実施の形態の半導体素子実装装置によれば、光半導体素子とプリアンプＩＣ等の半導体素子を回路基板両面に実装して、この基板間で電気的に信号ラインを接続し、かつ発熱する半導体素子を放熱筐体に熱的に接続することにより、回路基板上の素子実装効率を向上させ、また放熱も効果的に行えることから装置の小型化が図れる。さらに、光の影響を受けやすい半導体素子を完全に遮光することが可能となる。

【００４５】さらに、半導体素子とその半導体素子の周辺に配置すべき部品とを、回路基板の互いに反対の面に配置実装することにより、周辺部品を同一面上に配置実装する場合よりも近接して実装できる。これは特に、半導体素子が高速応答性を有する場合で、電源側の高周波デカップリング用のコンデンサを実装する場合に効果的である。

【００４６】（実施の形態３）図３は本発明の実施の形態３の半導体素子実装装置を示したものである。図１に示す実施の形態１と異なる点は、回路基板８１において、その基板内に光導波路１０２が形成されている点と、この光導波路１０２と光学的に接続する光ファイバ１０１を有している点と、ｐｉｎ－ＰＤ２１の受光面が、基板実装面の内側、すなわち放熱基台７に向かって設けられている点である。

【００４７】この場合、ｐｉｎ－ＰＤ２１に形成されたアンダーフィル１０は透明な樹脂、例えばシリコン系ゲル等を用いる必要がある。もしくはアンダーフィル１０を省いた構成としても良い。図３では光導波路１０２はｐｉｎ－ＰＤ２１の受光面に位置する場所で全反射機能を有し図面で光を上へ反射し、ｐｉｎ－ＰＤ２１の受光面に光を導くようになっている。また、回路基板８１も透明な材料で形成されており、例えばガラス系材料であればよい。このとき、回路基板８１上にＶ溝や凹溝のようなガイド溝を形成し、このガイド溝に光導波路１０２を配置するようにしてもよい。

【００４８】このように、本実施の形態の半導体素子実装装置によれば、光半導体素子への光結合系を回路基板内に内蔵させる構成とすることにより、光ファイバとｐｉｎ－ＰＤとの光学調整が実装する位置決めマーカによって行うことができ、装置作製工程の短縮が図れる。

【００４９】なお、光ファイバ１０１を放熱基台７に固定する場合には、放熱基台７に、例えばＶ溝や凹溝のようなガイド溝を形成しておけば、光導波路１０２を有す

る回路基板８１を放熱基台７上に固定する際のマーカとファイバ固定溝を兼用させることができ、調整固定が容易になる。

【００５０】なお、上記の説明において、放熱基台７に形成するガイド溝は本発明の第１ガイド溝に相当し、回路基板８１に形成するガイド溝は本発明の第２ガイド溝に相当するものである。

【００５１】（実施の形態４）図４は本発明の実施の形態４の半導体素子実装装置を示したものである。図２に示す実施の形態２と異なる点は、回路基板上に周辺部品１２、１３を配置する代わりに、回路基板８２内に、回路基板８２の材料よりも比誘電率の高い材料を回路基板８２の表面上に露出するように埋め込んで形成した領域１２０、１３０、及びｐｉｎ－ＰＤ２の実装面にも同様の材料で形成された領域１４１を有し、これらの領域１２０，１３０，１４１の対向する長手方向の面は導体電極で挟まれる形となっており、領域と電極とでコンデンサの機能を持たせるようにした点である。

【００５２】ｐｉｎ－ＰＤ２、プリアンプＩＣ３及び半導体ＩＣ４の電源（バイアス）供給端子にこのコンデンサが電気的に接続されており、コンデンサのもう一方の導体はグラウンドに接続されているため特に高周波領域のデカップリングに有効である。埋め込む高誘電率材料にはアルミナあるいはガラス系のセラミック材料で、比誘電率が１００以上あれば、図４のような構成で、層厚み０．１ｍｍ、１ｍｍ角の領域（層面積）で数ｐＦ以上の容量のコンデンサとして使用できる。

【００５３】また、さらに高誘電率材料、例えば比誘電率が１０００を越える材料を用いれば同一容量のコンデンサを同一厚みで形成する際に、埋め込み領域を小さくすることが可能である。また、容量の大きい（１０００ｐＦ以上）コンデンサも形成可能であることから低周波領域でのカップリングも基板埋め込み型のコンデンサで実現できる。

【００５４】ここで図６に、本実施の形態の回路基板に埋め込む誘電体およびその誘電体層を挟む電極の構成例をいくつか示す。図６（ａ）に示す構成は、回路基板１９０の表層部に誘電体層１５０が埋め込まれており、電極１６０及び１６１が誘電体層１５０を挟むように形成されている。ビアホール１８０及び１８１は電極１６１と回路基板裏面のパターンと接続されている。

【００５５】図４にも示したように、半導体素子３のバイアス供給ピンにこのビアホールの一方を接続させ、他方を回路基板８２裏面上のバイアス部に接続し、電極１６０を回路基板表面上のグラウンドに接続するようにすれば、電極１６０及び１６１に挟まれる誘電体層１５０はコンデンサとして機能する。

【００５６】図６（ｂ）は、本実施の形態の構成例として、誘電体層１５１が回路基板１９１の内層に形成されている例であり、この場合電極１６２及び１６３と回路基板１９１の表層上のパターンと接続するビアホール１８２及び１８３とを各々接続することにより、図６（ａ）に示す例と同様、コンデンサとしての機能を有することができる。この構成では回路基板１９１の表層上に誘電体層がないため、ビアホール１８２及び１８３の近傍に部品及びパターンを形成配置できる効果がある。

【００５７】また、図６（ｃ）は、図６（ａ）で電極１６１に接続されるビアホールが回路基板の同一面上に形成せず誘電体層１５２から延びた電極１６５とビアホール１８４とビアホール１８５とによって回路基板の両面にコンデンサの片方の電極を接続する構成である。これにより、例えばバイアス供給部の回路は回路基板１９２の表面上に形成することができる。

【００５８】次に図６（ｄ）は、広い誘電体層１５３の一部に複数の電極１６７と、１６８および１６９とを対向して配置する構成例である。これによりまず、電極１６７と電極１６８で挟まれる誘電体層で１つのコンデンサが、電極１６７と電極１６９で挟まれる誘電体層１５３でもう１つのコンデンサを形成できる。もちろんさらに並列的に電極を形成すれば多数のコンデンサを形成できる。図６（ｄ）の例では電極１６７を２つのコンデンサ機能の共通電極として利用しており、この部分をグラウンドに接続すればデカップリング用のコンデンサとして利用できる。もちろん電極１６７をそれぞれの部位毎に分離して形成すれば互いに独立したコンデンサとして利用できる。誘電体層の厚みや領域の大きさで容量を変化させることができる為に、特に高周波回路用の基板として用いることにより、装置の小型化と共に伝送線路容量の低減が図れ、望まれる高周波特性を素子実装後も確保する事ができる。

【００５９】なお、図１から図４、図７，図８に示す各実施の形態においては、本発明の光半導体素子の一例として受光素子であるｐｉｎ－ＰＤについて示したが、これは例えばアバランシェフォトダイオード（ＡＰＤ）でも良い。また、光半導体素子として半導体レーザを用いてもよい。ここで示した例に適用するためには面発光型で放射角の小さい半導体レーザを用いるのが望ましい。この場合プリアンプＩＣ２はレーザドライバＩＣとなり、より発熱が大きくなるため、筐体への直接的な放熱ができる本構成が有効である。

【００６０】また、上記各実施の形態においては、半導体素子と光半導体素子とを備えた構成として説明を行ったが、本発明は、半導体素子だけを有する構成としても良い。この場合、放熱効率と実装効率とを向上させることが可能となる。

【００６１】また、回路基板８，８１、８２と放熱基台７との接続固定には、金属製ねじによる固定あるいははんだ固定により確実な電気的接続が可能である。

【００６２】さらに回路基板８，８１、８２と放熱基台７の熱膨張係数の差異による接続固定部への応力印加が

懸念される場合は、導電性接着剤を用いた接続により樹脂層での応力緩和により接続安定性が図れる場合がある。

【００６３】また、回路基板８，８１、８２に実装される光ファイバ及び光導波路や光半導体素子、半導体素子は放熱性良く実装されているため、絶縁性樹脂によって全てモールドするような構成（図示せず）を行っても熱滞留が無く、かつ外部からのダスト等の混入を防止し動作の長期安定性を確保することができる。

【００６４】また、放熱基台７の材料としては、高周波特性を向上させるためには、充分な接地を確保できるものが望ましく、金属などの、導電性および熱伝導性のいずれにもいてもすぐれた材料が望ましく、例えば、銅、アルミニウム等を用いればよい。

【００６５】また、回路基板８，８１、８２等の材料としてセラミック基板を用いる場合には、回路基板と放熱基台との間の熱膨張率の差異を補正するため、放熱基台７の表面（回路基板８，８１、８２との接面）にコバールを配置し、これに膨張率の差異に基づくひずみを吸収させるようにするか、回路基板と放熱基台との間の熱伝導性を阻害しない程度に薄い導電性樹脂を介して接続するようにすればよい。

【００６６】加えて上記実装装置を用いた光受信装置あるいは光送信装置で構成させる光通信装置は、放熱効果に優れ、放熱基台を筐体と一体化できることから実質的に放熱面積が増大し、放熱効果をより大きくできると共に、変調手段、送信手段を備えた場合は光送信機として、また復調手段、受信手段を備えた場合は光受信機として動作する光通信装置として小型化できる効果を有する。

【００６７】

【発明の効果】以上のように構成された本発明は、半導体素子を回路基板両面に実装して、この基板間で電気的に信号ラインを接続し、かつ発熱する半導体素子を放熱筐体に熱的に接続する構成とすることにより、回路基板上の素子実装効率を向上させ、また放熱も効果的に行え＊ることから装置の小型化が図れる。

【００６８】さらに半導体素子とその半導体素子の周辺に配置すべき部品を回路基板の互いに反対の面に配置実装したり誘電体層を回路基板上または回路基板内に埋め込み電極を接続することにより、同一面積の回路基板上での部品実装効率を上げ、装置としてさらに小型化できる。これは特に、半導体素子が高速応答性を有する場合で、電源側の高周波デカップリング用のコンデンサを実装する場合に効果的である。

【図面の簡単な説明】

【図１】本発明の実施の形態１の半導体素子実装装置の図式的断面図

【図２】本発明の実施の形態２の半導体素子実装装置の図式的断面図

【図３】本発明の実施の形態３の半導体素子実装装置の図式的断面図

【図４】本発明の実施の形態５の半導体素子実装装置の図式的断面図

【図５】従来の半導体素子実装装置の図式的断面図

【図６】誘電体層埋め込み回路基板の構成例を示す図式的断面図

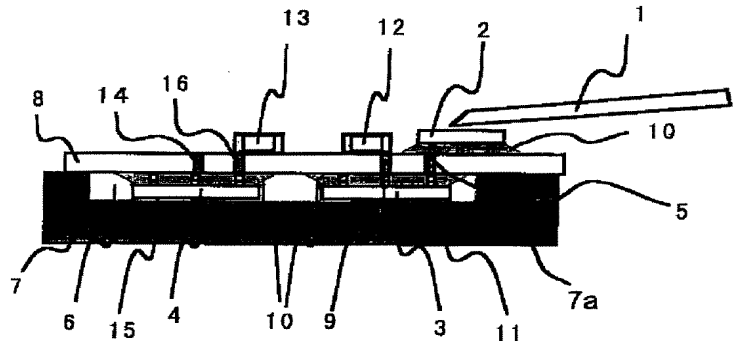
【図７】本発明の実施の形態１の半導体素子実装装置の他の構成例を示す図式的断面図

【図８】本発明の実施の形態１の半導体素子実装装置の他の構成例を示す図式的断面図

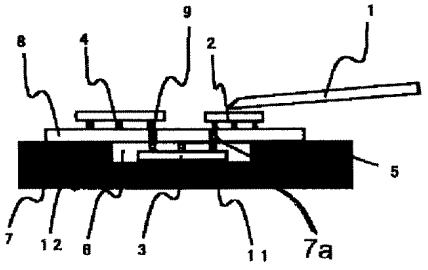
【符号の説明】

１、１０１　光ファイバ
２　ｐｉｎ－ＰＤ
３、４　半導体素子
５，９，１４，１６　ビアホール
８、８１　回路基板
７　放熱基台
７ａ　凹部
１０２　光導波路
１２０、１３０　誘電体層

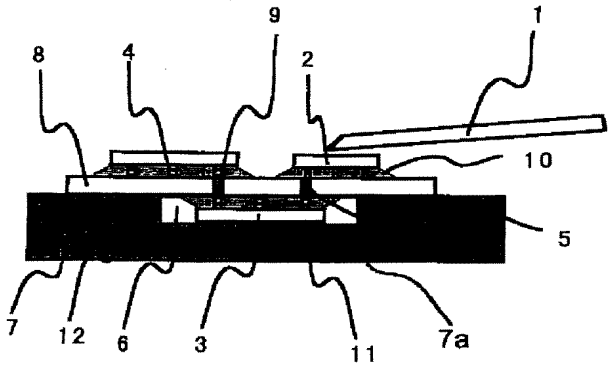
【図２】



【図７】

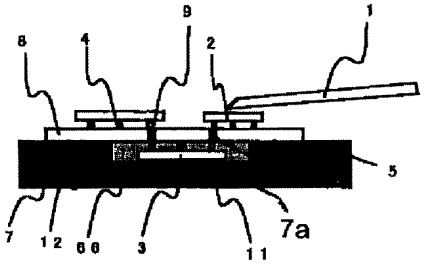


【図１】

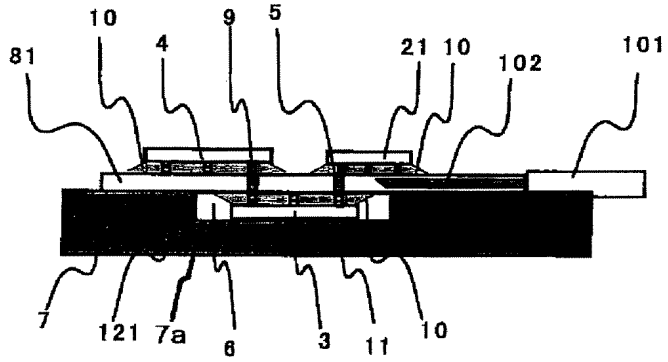


1:光ファイバ　　5、9:ビアホール　　8:回路基板
2:pin－PD　　6:開口　　10:アンダーフィル
3、4:半導体素子　　7:放熱基台　　11:放熱面
7a:凹部　　12:周辺部品

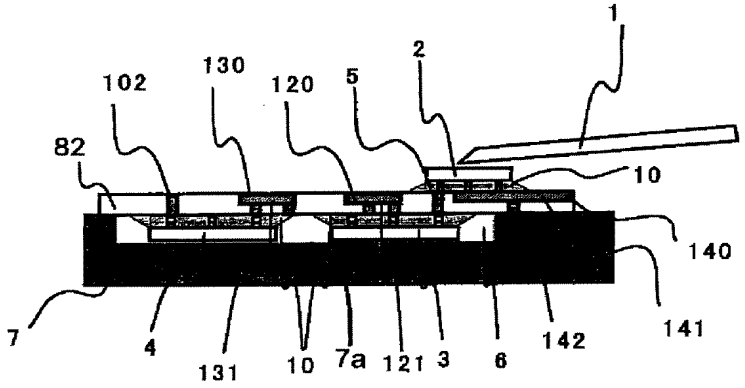
【図８】



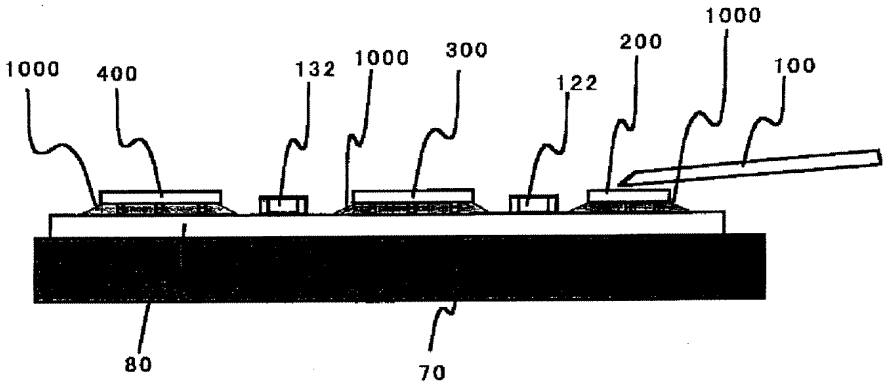
【図３】



【図４】



【図５】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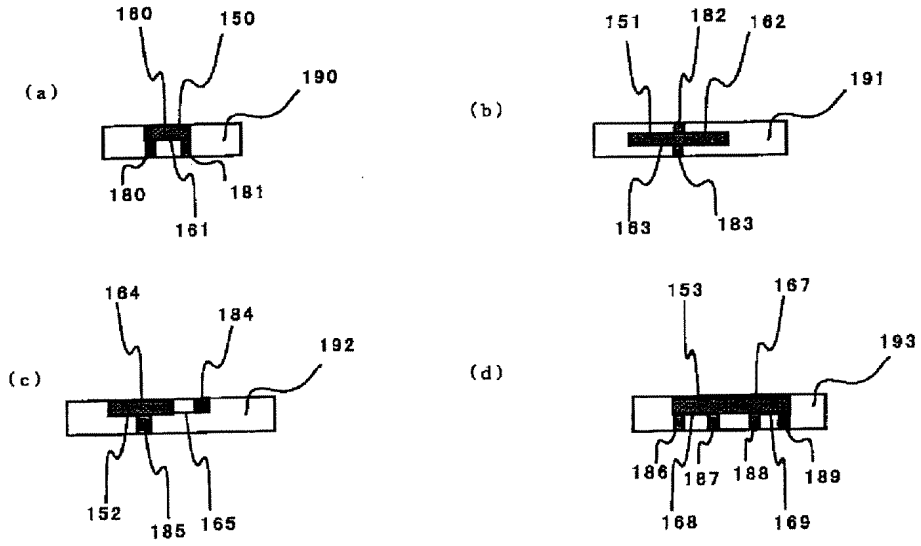
1000
100
80
70

【図６】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161
(b)
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183
(c)
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(d)
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